ABSTRACT

Methods and apparatus are provided for achieving low latency for high priority tasks in digital processing systems. A digital signal processor includes a core processor and a level one memory. In some embodiments, a store buffer is configured to hold write information for the level one memory and for a level two memory. A write buffer is configured to hold write information, received from the store buffer, for the level two memory. The write buffer has a normal capacity and an excess capacity. A memory controller enables the excess capacity of the write buffer when a high priority task is being serviced and inhibits write access to the excess capacity of the write buffer when a high priority task is not being serviced. In other embodiments, the digital signal processor includes first and second fill buffers configured to hold read data in a fill operation. The memory controller steers low priority read data to the first fill buffer or the second fill buffer based on priority of the fill operation.